

राष्ट्रीय प्रौद्योगिकी संस्थान, उत्तराखण्ड
NATIONAL INSTITUTE OF TECHNOLOGY, UTTARAKHAND

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WALK-IN-INTERVIEW

(Advt. No. 04/2025 Date: 05 /02/2025)

With reference to the advertisement No. 04/2025;dated 05/02/2025,Walk-In-Interview (Hybrid Mode) shall be conducted for the position of Junior Research Fellow/Research Associate-I/ Research Associate-II/ Research Associate-III for the project titled "VLSI Design and Implementation of Imagined Speech based Neuroprosthesis: An Application in Healthcare System" funded under Chips to Startup (C2S) Programme, MeITY, Govt. of India under the supervision of Dr. Hariharan Muthusamy, Principal Investigator in the Department of Electronics Engineering, NIT Uttarakhand. The details of post, essential qualifications and fellowship are as under:-

Designation of post	Essential qualifications	Fellowship	Number of post	Tentative date and Time of Walk-in interview
Junior Research Fellow OR	M.E/M.Tech./M.S in Microelectronics and VLSI Design/Communication Systems/Biomedical Engineering/Digital System and Signal Processing/Instrumentation and Signal Processing/ Signal Processing and Control/Electronics and Communication Engineering/Communication and Signal Processing/Digital Signal Processing/ Signal Processing or allied areas with minimum of 1 st class in B.E/B.Tech & M.E/M.Tech./M.S In addition GATE/CSIR-UGC NET including lectureship(Assistant Professorship) is mandatory. Age: Preferably below 35 Years	Rs. 37,000/- pm + HRA as per norms	01	Walk-in interview 03/03/2025 (Monday) at 03.30 PM Reporting Time 02.00 PM to 03.30 PM
Research Associate – I OR	Ph.D in Microelectronics and VLSI or Signal Processing or M.E/M.Tech having 3 years of research, teaching and design and development experience with at least one research paper in SCI journal Age: Preferably below 45 Years	Rs. 58,000/- pm + HRA as per norms		
Research Associate – II OR		Rs. 61,000/- pm + HRA as per norms		
Research Associate – III		Rs. 67,000/- pm + HRA as per norms		

***The Institute may decide the level in which a particular associate should be placed based on the experience.**

Skill requirements

- Knowledge of Custom/ASIC/FPGA based VLSI design and EDA tools
- Knowledge of MATLAB, Hardware Description Language and Python programming
- Good Technical and Communication Skills.

Interested candidates shall appear for walk-in interview along with application form, all originals and self-attested photo-copies of relevant certificates as per the above schedule at Committee Room (C106), Department of Electronics Engineering, NIT Uttarakhand, Temporary Campus - Govt. ITI, Srinagar Garhwal - 246174. Candidates are urged to send the advance copy of completely filled application form and relevant certificates via email to hariharanm@nituk.ac.in in the subject line please specify **"Application for Junior Research Fellow/Research Associate-I/ Research Associate-II/ Research Associate-III position in C2S project"**

General Terms & Conditions:

1. The duration of post will be initially for one year and which may be extended upto the duration of project based on the satisfactory performance. The fellowship may be terminated if performance of candidate is not satisfactory.

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2. The post created under the C2S Programme, MeiTY project is purely on temporary basis and neither MeiTY nor the Institute would have liability whatsoever for sustaining temporary staff recruited under the above mentioned project, after its completion/termination.
3. Only those candidates who are present before the reporting time on scheduled date will be considered for Interview. **Candidates reporting after the scheduled reporting time for document verification shall NOT be eligible to appear for the Interview.**
4. The Junior Research Fellow and Research Associate-I/II/III with M.Tech/M.E will have option to register for Ph.D. program of institute; the candidate must meet the essential qualifications and qualify written examination & interview of Ph.D. admission of institute.
5. NIT Uttarakhand has right to cancel the recruitment for the aforesaid post at any time without providing any clarifications/information.
6. No interim correspondence will be entertained and canvassing in any form will lead to disqualification.
7. No TA/DA will be paid for attending the Walk-In-Interview.

-Sd-
Registrar

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DEPARTMENT OF ELECTRONICS ENGINEERING

Application form for the post of Research Associate I/II/III or Junior Research Fellow in research project

1. Name in full
2. Father's / Husband's name
3. Date of Birth
4. Nationality
5. Gender
6. Category
7. Mobile number
8. Email id
9. Address for correspondence:

Paste
Passport size
Photo

10. Permanent address:

11. Detailed educational qualification in chronological order starting from 10th standard :

Degree	Specialization	Name of University/Institute	% of Marks or CGPA obtained	Class/Division	Year of passing

12. Ph.D Thesis title:



14. GATE/NET-JRF qualified: YES/No

(Original certificates and Self-attested photo-state copies should be produced at the time of interview).

Name of Examination	Year of Passing	Validity Period	Number of candidates appeared	Marks obtained	AIR Rank	Score / Percentile

16. Publications (if any)

17. Any other relevant information (max. 100 words)

Declaration

I certify that the above information is correct and complete to the best of my knowledge and belief and nothing has been concealed /distorted. If at any time I am found to have concealed / distorted any material/information, my engagement shall be liable to be summarily terminated without/notice/compensation.

Place:

Date:



(Signature of Candidate)